ABSTRACT

Communication in a System-on-Chip Virtual Machine

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With the increasing complexity of hardware designs and the rise in the use of embedded software, ASIC technology has moved away from the chipset philosophy to that of a system-on-chip (SoC) philosophy. System-on-Chip is the integration of multiple standalone intellectual property (IP) cores into one integrated circuit.

Virtual machines have increased in popularity as many different hardware platforms have been brought together by the use of the Internet. Virtual machines provide the ability for software to be written once and run anywhere because virtual machines abstract the physical hardware platform away from the software. However, virtual machine applications have the disadvantage of running significantly slower than native applications.

The co-designed virtual machine helps improve execution speed by providing a hardware execution engine that works alongside the software virtual machine to execute virtual machine instructions natively. This work focuses on interfacing the hardware execution engine to software running on a PowerPC processor embedded within a Field Programmable Gate Array (FPGA) device. The execution engine is connected to the PowerPC through an IBM CoreConnect bus making this a complete system-on-chip design.

The goal of this research is to increase performance while investigating the increase in communication between hardware and software. Communication speed between hardware and software has been a problem in co-designed virtual machines, but by bringing the hardware and software into the same chip, the communication speed can be increased, providing better performance for the virtual machine. This technique can also be applied to others systems to increase performance when needed.