An Extensible Virtual Machine Using a Network-on-Chip Design

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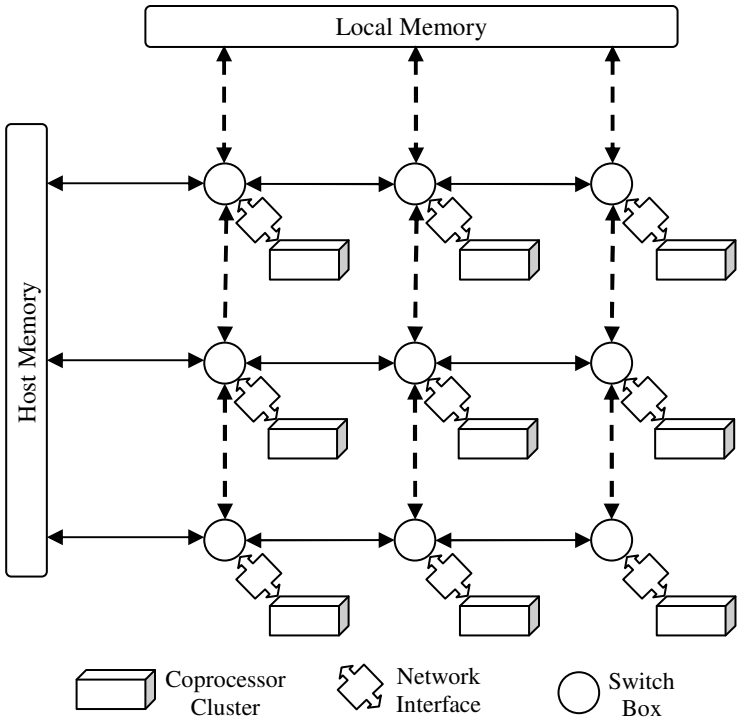
ABSTRACT

In accordance with Moore's law, transistor sizes have been reduced at a rate of doubling memory capacity per unit area every 18 months over the past 40 years, and this trend is expected to continue several more years. This allows for more functionality to be integrated into a single chip, by bringing together multiple components (e.g., Digital Signal Processor cores, memory blocks). When many components are put together, however, communication between each piece often becomes performance bottleneck. This defect can be mitigated by utilizing structured communication rather than direct connections between components. This work presents the design and implementation of a prototype that integrates multiple Java Virtual Machine coprocessors into a single hardware device, using a Network-on-Chip (NoC) design methodology. Each coprocessor core requires access to certain components that are shared with other cores (such as a common Floating Point Unit, or shared memory). Results show that factors such as whether data can be split up and processed by separate threads, the available hardware space, and desired performance improvement are all key considerations when designing a NoC.



NoC Architecture