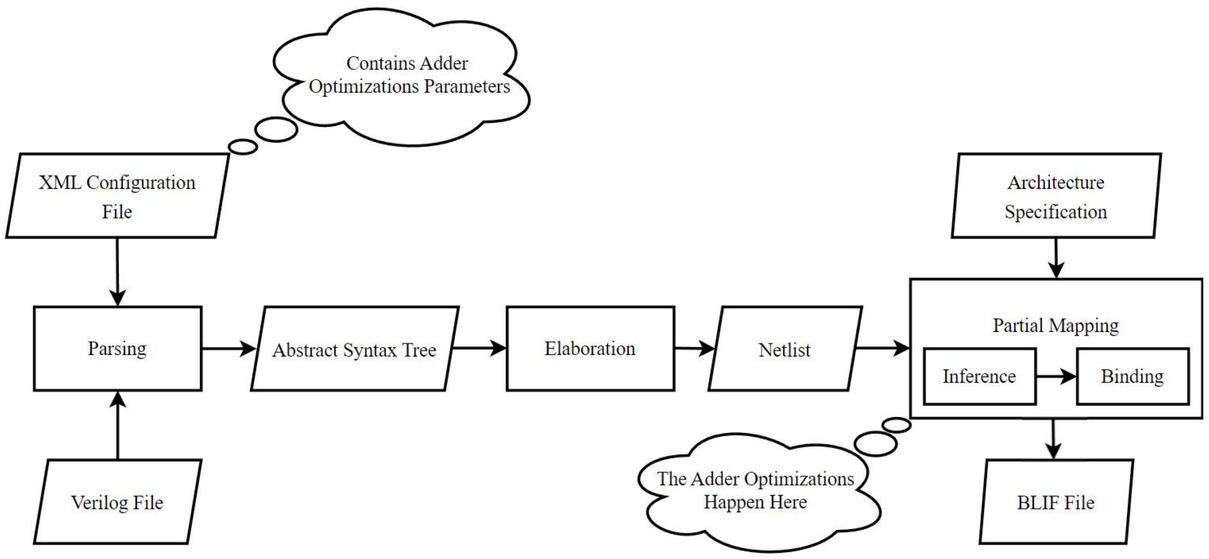
Heterogeneous Logic Implementation for Adders in VTR

Navid Jafarof, Kenneth B. Kent
Faculty of Computer Science, University of New Brunswick
navid.jafarof@unb.ca - ken@unb.ca

Introduction

VTR is an open-source tool that can be used for researching FPGA architectures and CAD. It supports the examination of new FPGA designs not possible with proprietary software. This tool takes in a Verilog circuit description and generates FPGA performance results, which include critical path delay, and size results in terms of area, through various stages such as Elaboration and Synthesis (ODIN II), Logic Optimization, Technology Mapping (ABC), Packing, Placement, Routing, and Timing Analysis (VPR).

ODIN II has the advantage of incorporating both soft logic adders and hard block adders, which is useful when there are insufficient hard blocks available for addition. Research has demonstrated that adder optimization techniques can improve performance by up to 23% regarding critical path delays.

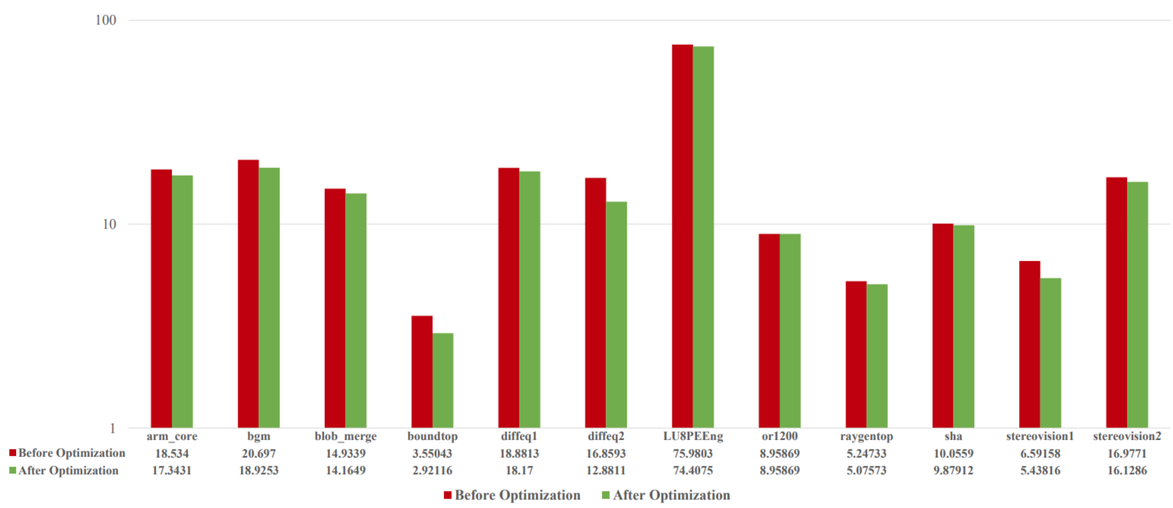


- Combining hard and soft logic blocks to overcome limitations caused by a lack of hard blocks
- Introducing new attributes and functionalities to ODIN II to support the optimization of adders
- Improving performance regarding critical path delays

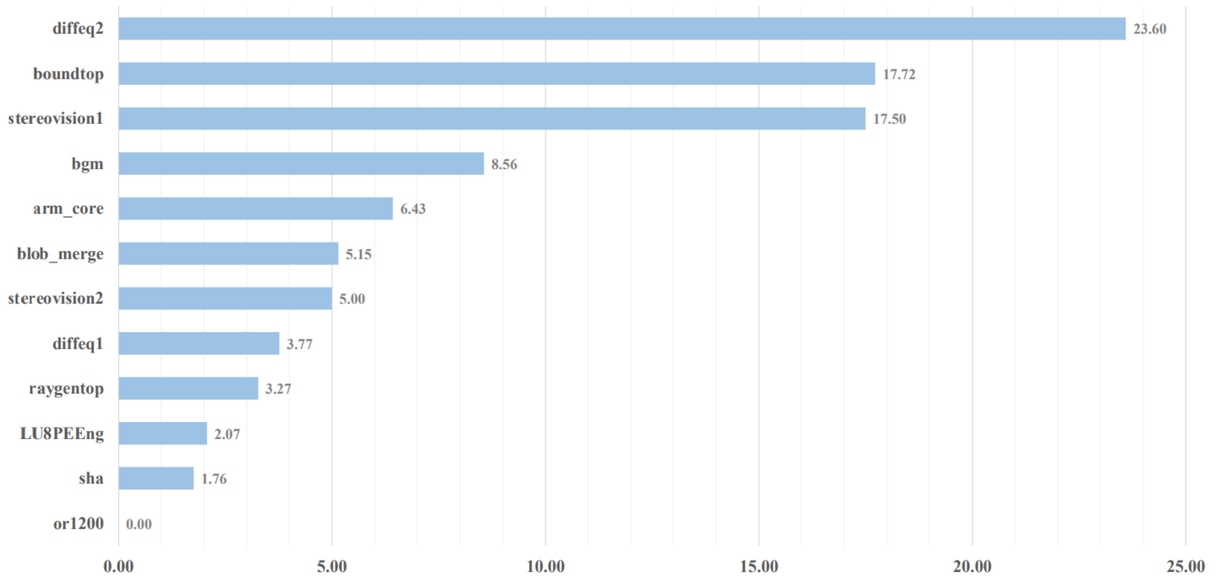
Circuit / Adders Ratio	0%	5%	10%	15%	20%	25%	30%	35%	40%	45%	50%	55%	60%	65%	70%	75%	80%	85%	90%	95%	100%
arm_core	18.58	18.89	18.04	17.34	18.17	18.36	18.79	17.89	18.60	17.81	17.71	18.85	19.61	18.12	18.97	19.42	19.35	19.69	18.56	18.94	18.53
bgm	19.90	19.69	18.93	20.66	19.32	21.44	19.76	20.71	19.78	20.84	20.83	20.80	20.20	19.40	21.30	21.14	20.90	20.32	20.15	20.51	20.70
blob_merge	14.61	14.64	15.50	14.16	15.10	15.94	15.17	14.86	16.30	15.25	15.32	15.45	15.37	15.49	15.78	15.65	14.97	15.58	15.56	15.46	14.93
boundtop	3.01	3.25	3.53	3.62	3.22	3.67	3.44	3.39	3.51	3.11	3.13	3.42	3.38	3.51	3.10	2.92	3.12	3.61	3.55	3.55	3.55
diffeq1	18.66	18.17	18.17	18.17	18.17	18.17	18.88	18.88	18.88	18.88	18.88	18.88	18.88	18.88	18.88	18.88	18.88	18.88	18.88	18.88	18.88
diffeq2	13.14	13.44	13.44	13.44	13.44	13.44	12.88	12.88	12.88	12.88	12.88	13.51	13.51	13.51	13.51	13.51	16.86	16.86	16.86	16.86	16.86
LU8PEEng	76.27	76.64	75.04	75.31	76.72	75.04	75.97	78.30	75.74	75.23	74.93	76.13	74.41	78.49	74.66	76.25	76.67	77.40	76.80	76.55	75.98
or1200	15.14	17.20	15.35	15.35	15.08	15.08	14.96	14.96	14.78	14.78	14.71	9.24	9.24	9.56	9.56	9.25	9.25	9.16	9.16	8.96	8.96
raygentop	6.24	5.67	6.24	5.25	5.08	5.45	5.78	5.57	8.24	5.33	5.80	5.57	5.72	5.26	6.38	5.20	5.17	6.71	5.66	5.74	5.25
sha	14.66	14.53	14.53	15.43	15.43	14.82	14.82	14.46	14.46	15.02	15.02	10.33	10.33	10.25	10.25	9.88	9.88	11.87	11.87	10.06	10.06
stereovision1	6.30	6.37	5.44	6.72	5.46	6.02	8.69	5.72	5.47	5.58	5.90	5.45	6.35	6.96	6.74	6.77	6.16	6.93	6.95	5.73	6.59
stereovision2	17.43	17.71	18.26	18.32	19.08	16.67	18.19	18.21	17.68	17.86	17.58	17.79	18.07	18.76	18.67	17.63	16.35	17.64	16.91	16.13	16.98

Heat Map Visualization of CPDs For a Range of Optimizations
The Greener, The Better

Results



CPD of Circuits Before and After Optimizations in Nanoseconds
The Lower, The Better



Percentage CPD Gain Chart

Contributions

- Finalizing the feature, involving fixing bugs and ensuring that software passes QoR tests
- Generating new results according to the changes made in the software
- Verification and validation of the new results
- Merging the finalized software with the public repository

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