Faculty of Computer Science UNB

FACULTY OF COMPUTER SCIENCE

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Functional Coverage in Bounded Model Checking

By

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Formal verification has become an important step in circuit and system design. One prominent technique in this context is model checking. Model checking is an automatic method for verifying that a finite-state system satisfies a temporal property. Since the classical approaches suffer from state explosion, methods based on Boolean Satisfiability (SAT) have been proposed. In Bounded Model Checking (BMC), the system is unfolded for k time frames and together with the property converted into a SAT instance. BMC can be applied to large designs and is widely used in the industry.

However, even if all the specified properties can be verified, it is difficult to determine whether they cover the complete functional behavior of a system. In this talk an approach to analyze functional coverage in BMC is presented. The approach is demonstrated for the complete formal verification of a RISC CPU. During the verification coverage gaps have been identified. All of them have been closed and 100% functional coverage is achieved.

STUDENTS ARE ENCOURAGED TO ATTEND