2009/2010 Seminar Series



"Odin-II: Building a Compiler for Exploring FPGA Architectural Designs" by Dr. Ken Kent

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The primary goal of recent FPGA architecture research is in adding dedicated "hard" logic to accelerate common functionalities. Some of these dedicated hard logic elements include multipliers and memories. To effectively evaluate a Field Programmable Gate Array (FPGA) device, one must test proposed architectural designs with benchmark circuits. This requires a complete software CAD flow to support the proposed FPGA.

In this talk, I will give an overview of the complete CAD flow. That is being developed and some details of the front-end compiler (Odin-II). Preliminary research results will be presented, but in most cases open problems exist rather than solutions.

Monday, December 7th @ 3:30pm Information Technology Center, C-317