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Formal Specification Level

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Abstract: The steadily increasing complexity of the design of embedded systems led to the development of both an elaborated design flow that includes various abstraction levels and corresponding methods for synthesis and verification. However, until today the initial system specification is provided in natural language which is manually translated into a formal implementation e.g. at the Electronic System Level (ESL) by means of SystemC in a time-consuming and error-prone process.

In the talk, we envision a design flow which incorporates a Formal Specification Level (FSL) thereby bridging the gap between the informal textbook specification and the formal ESL implementation. Modeling languages such as UML or SysML are envisaged for this purpose. Recent accomplishments towards this envisioned design flow, namely the automatic derivation of formal models from natural language descriptions and verification of formal models in the absence of an implementation are briefly reviewed.

Bio: Mathias Soeken received the Dr.-Ing.degree in Computer Science from the University of Bremen in 2013. Since 2009, he is with the Group of Computer Architecture at the University of Bremen and, since 2012, with the German Research Center for Artificial Intelligence (DFKI). His research interests are in electronic design automation, formal verification, natural language processing, and circuit complexity. Since 2012, Mathias Soeken teaches graduate courses on reversible logic and quantum computing at the University of Bremen.

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