2012/2013 Seminar Series

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Evaluation of Data Transfer from FPGA to PC: Increasing Frame Rate by BLOB Detection

By:

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This work presents a novel hardware/software codesign approach to blob detection. Camera images are preprocessed on a field-programmable gate array that separates foreground pixels from the background. The foreground pixels are transferred to the PC over a 100 Mbit/s Ethernet interface by using a custom protocol. The PC reconstructs the images from received foreground pixels and extracts centers of masses from every blob in the image. Results of evaluation show that under the constraint of 100 Mbit/s the FPGA is able to transmit a large amount of blobs if their sizes are small enough.

Peter Samarin is a graduate student in Master of Autonomous Systems at the Bonn-Rhine-Sieg University, Sankt Augustin, Germany. He is currently working on his master's thesis with the purpose of developing a system that detects a grid of fiducial markers at high speed by using an FPGA. Peter has a bachelor's degree in computer science

Wednesday, November 28 @ 3:30pm
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