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Verification Tasks at the Formal Specification Level

By: Nils Przigoda

The complexity of modern embedded or pure hardware systems makes it inevitable to consider higher abstraction levels in the design process to overcome problems in an acceptable time with an acceptable effort. To solve this problem, in the last years the so-called Formal Specification Level (FSL) has been proposed. In the FSL modeling languages such as UML or SysML are used for describing system at a very abstract level for first verification tasks. In the talk, general verification tasks will be introduced and it will explained how they are translated into a satisfiability problem (SAT/SMT) in order to obtain first results for the desired system. Some ideas for debugging inconsistent models will be explained in detail, before some open questions will be presented.

Nils has started to study mathematics with computer science as a secondary subject in 2006 at the University of Bremen (Germany). In 2009 he decided to also study computer science towards a master degree. After attending a 2 year project on reversible logic and quantum computing, he also wrote his master thesis in this area and obtained the degree in March 2013 in mathematics and another one for computer science in June 2013. Since April 2013 he is a PhD candidate in the group of computer architecture at the University of Bremen under the supervision of Rolf Drechsler. For his PhD he switched the research field to "formal verification of UML models", but if there is some time left, he still thinks about reversible logic problems.

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